PROGRAMMABLE MASK ROM BUILDING ELEMENT
AND PROCESS OF MANUFACTURE

5   REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of the priority
date of German application DE 102 54 155.8, filed on
November 20, 2002, the contents of which are herein
10   incorporated by reference in their entirety.

                  FIELD OF THE INVENTION

15   The invention pertains to a semiconductor memory
component, for example, a read-only memory component,
and more particularly to a mask-programmable ROM
component, and to a process for the production of such
a ROM component.
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                  BACKGROUND OF THE INVENTION

Semiconductor memory devices, that is, semiconductor
components with at least one memory cell, are used to
25   store data in digital systems. In correspondence with
the type of data storage and the various ways in which
the data can be written and read out again, these
semiconductor memory devices are divided into various
categories. If the memory device continues to store
30   the information even after the supply voltage has been
turned off, the device is a non-volatile memory (read-
only memory), such as a ROM device. The category of
volatile memory devices includes static and dynamic
memories such as SRAM (Static Random Access Memory) and
35   DRAM (Dynamic Random Access Memory). After production,
data can be freely written to and read from these

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volatile memory components. In contrast, data cannot usually be written to the non-volatile memory components after they have been produced, and they are therefore used essentially only as sources from which

5   data can be read.

Read-only memories (ROM's) are used in digital systems to store constants, control data, and program instructions. The information is stored by providing

10   transistors at the intersections between the word lines and the bit lines to connect the word lines to the bit lines or by not providing any transistors there so as not to connect the two types of lines. These MOS (Metal Oxide Semiconductor) transistors are arranged in

15   the form of a matrix in a memory field region of the ROM component.

The cells for a MOS-ROM component (Metal Oxide Semiconductor Read-Only-Memory) require only one

20   transistor to store a bit. In one possible design, namely, that of an n-channel transistor, the source region is connected to ground ("low potential"). To store a bit ("high" or "low" potential), an electrical contact is placed in the drain region of the transistor

25   to establish an electrical connection between the transistor and the bit line (BL). When the word line (WL), which represents the gate of the transistor, is now opened, "low potential" can flow from the source region to the drain region and can be read via the bit

30   line. As a result, the 1-bit ROM memory cell is programmed to the logical state "0". To program the "high potential", the electrical contact between the drain region of the transistor and the bit line is

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omitted.   The bit line is therefore undefined, and the
1-bit ROM memory cell is programmed to the other
logical state "1".

5   In accordance with the complexity of the system, the
memory requirement can range from only a few bits to
many billions of bits.   If relatively little memory is
required, the memory devices are integrated as modules
into a chip along with the data paths and control
10   logic.   If it is necessary to store large amounts of
data, standardized units are produced.   The criteria
under which standard memory units are evaluated are
cost (and thus complexity), speed of access to the
data, power loss, and reliability.
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Read-only memories or ROM components differ with
respect to whether the data are written into them by
electrical pulses during the production process or
after production.   The ROM components considered within
20   the scope of the state of the art, in which the data
are written into the devices during production, are
called "mask-programmable ROM components".   Depending
on the method used to encode the data during
production, mask-programmable ROM's can be either of
25   the diffusion type, of the contact type, or of the via-
contact type.

For ROM's of the diffusion type, programming is carried
out by forming or omitting transistors at the
30   intersections between the word lines and the bit lines
in correspondence with the data to be stored.   The
encoding or programming therefore takes place at a very
early stage of the production process.   For this type

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of ROM, many additional process steps are required
after programming to finish the memory component, and
as a result the "turn-around-times" are long. The
turn-around-time is the time the customer must wait for
5   delivery of the finished product after he has provided
the manufacturer with his specifications for the
desired mask-programmable ROM.

In ROM's of the contact type, the memory cells are
10   programmed by creating or leaving out the electrical
contacts between the memory cell transistors and the
bit lines located in the first metallization plane
above the memory cell transistors. In the via-contact
type, the programming is shifted to a higher
15   metallization plane. Because of the different
arrangements of the word lines and bit lines required
in the via-contact and contact types, however, the
amount of surface area required is greater than that
for the diffusion type. The data in these memory
20   components known as "mask-programmable ROM's" cannot be
erased or overwritten.

In the case of mask-programmable ROM's, it is
especially desirable to minimize the so-called "turn-
25   around-time" (TAT) or "cycle time". Efforts are always
being made to reduce this turn-around-time. At the
same time, it is desirable to minimize the amount of
space required by the memory cells.

30   A mask-programmable ROM component is disclosed in U.S.
Patent No. 5,959,877, in which the programming can be
carried out in the second, third, or a higher
metallization plane. The transistors are arranged in

the form of a matrix in the memory cell field, thus
forming rows and columns. The transistors arranged in
one row are connected to the same word line. The
transistors arranged in adjacent columns are connected
5   by their gate terminals to different word lines. Only
the diffusion regions of the two outer transistors of a
column, i.e., the diffusion regions facing the edge of
the memory cell field, are connected to ground
potential. All of the other diffusion regions, each of
10   which is assigned to two transistors, can be contacted
by the bit lines situated above them. The transistors
are therefore connected in series between the
potentials of the word lines, and the diffusion regions
of adjacent transistors are connected to several
15   potential nodes. Although it is true that the cycle
time can be kept relatively short by shifting the
programming into a higher metallization plane, this
wiring design requires a very large amount of space to
accommodate the complicated configuration and layout of
20   the word lines and bit lines.

In the case of mask-programmable ROM cell fields, word
lines are usually produced out of polysilicon. Because
polysilicon lines have a high resistance value, it is
25   advantageous to amplify the signals on these
polysilicon lines or to adjust them to the required
signal strength by means of an additional line in one
of the metallization layers, especially when the memory
cell field has a very large number of memory cells and
30   it is therefore impossible to avoid a drop in the
potential along the transistors connected to one word
line.

An arrangement of lines of this type for row selection
and potential equalization is shown in Figure 1.
Figure 1 shows two memory cell transistors, which are
arranged next to each other in a column of a memory

5   cell field. The first memory cell has a first memory
cell transistor, the gate G1 of which is connected to a
first word line W1. Via its drain terminal D1, this
first memory cell transistor is contacted by a bit line
BL, i.e., programmed to the first state, by way of a

10   contact K, a first contact path P1 in a first
metallization plane, a first via connection V1, a
second contact path P2 in a second metallization plane,
and a second via connection V2. A source region 50 is
assigned to the first and to the second memory cell

15   transistor. The second memory cell transistor is
designed in the same way as the first memory cell
transistor. The separating lines TL designate the
boundaries of a memory cell and characterize the unit
cell.

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To equalize the mass potential, to which the source
region 50 is connected, a ground potential equalization
line PAM is provided, with which the source region 50
can be brought into contact. For row-select/potential-

25   equalization, each memory cell has its own electrical
row-select/potential-equalization line PAW1 or PAW2,
where the two row-select/potential-equalization lines
PAW1 and PAW2 are formed in a metallization plane above
the bit line BL. These row-select/potential

30   equalization lines PAW1 and PAW2 are therefore produced
only after the memory cells have been programmed, which
has the effect of prolonging not only the process of

producing the mask-programmable ROM's but also the
overall cycle time.

SUMMARY OF THE INVENTION

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The task of the invention is to create a semiconductor
component and a process for its production according to
which both the amount of space required and the turn-
around-times are minimized. In particular, programming
10   is to be done in the latest possible stage of the
production process, while at the same time the
arrangement of the word lines and bit lines, especially
the row-select/potential-equalization lines, is to be
optimized.

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A semiconductor memory component according to the
invention has a first and a second memory cell
transistor and a first and a second row-
select/potential-equalization line. The first memory
20   cell transistor is electrically connected to a first
selection line, and the second memory cell transistor
is electrically connected to a second selection line.
One aspect of the invention is that the first row-
select/potential-equalization line and the second row-
25   select/potential-equalization line are arranged
vertically with respect to each other, between the two
memory cell transistors. The semiconductor memory
component is designed in one example as a ROM
component, such as a mask-programmable ROM (Read-Only
30   Memory) component. As a result of the arrangement
according to the invention of the two row-
select/potential-equalization lines, the amount of
space required by the component can be significantly
reduced. In that the row-select/potential-equalization

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lines are at different distances in the vertical
direction from the memory cell transistors, the memory
cell field and thus also the semiconductor memory
component can be significantly reduced in size.

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In one exemplary embodiment, at least one of the two
row-select/potential-equalization lines is equidistant
from the two memory cell transistors or from the
selection lines, which are designed in particular as
10   the first and second word lines. As a result, the row-
select/potential-equalization line can be assigned to
two memory cell transistors adjacent to each other in
one column of a memory cell field. At least one of the
two row-select/potential-equalization lines is
15   therefore equidistant from the two memory cell
transistors. As a result of this optimized arrangement
of the first row-select/potential-equalization line, it
also becomes possible to optimize the arrangement of
all the other electrical lines required for the overall
20   memory component, specifically the data lines and the
word lines. In particular, these other required
electrical lines can be laid out in such a way that the
programming of the semiconductor memory component can
be carried out at a relatively late point in the
25   overall fabrication process.

In another exemplary embodiment, at least one of the
two row-select/potential-equalization lines is arranged
essentially vertically above and centered over a
30   diffusion region of the memory cell transistors. This
diffusion region, above which at least one of the row-
select/potential-equalization lines is located, is
assigned to both the first and the second memory cell

transistor. As a result, it is a simple matter to establish contact with the first or with the second memory cell transistor or with the word lines.

5   It is especially advantageous for the first and the second row-select/potential-equalization line to be arranged one above the other, so that they are essentially coincident in the vertical direction. The amount of space required for the memory cell can thus
10   be reduced in an especially effective manner, because, in practice, the area which can be eliminated in the case of two adjacent memory cell fields will always be that area – as seen when looking down onto the memory cell field from above – which would have to be provided
15   on the basis of the applicable design rules between the two row-select/potential-equalization lines if they were to be arranged horizontally next to each other (as in the state of the art).

20   It is also advantageous for the two row-select/potential-equalization lines to be provided in different metallization planes.

It is possible, in one exemplary option, for the first
25   row-select/potential-equalization line to be provided in the second or the third metallization plane above the first and the second memory cell transistor. The second row-select/potential-equalization line would then be formed accordingly in the third or second
30   metallization plane. An especially space-saving design can be obtained by arranging the two row-select/potential-equalization lines vertically one

above the other so that they are symmetrical to the two
memory cell transistors in one column.

It is advantageous for the first or the second row-
5   select/potential-equalization line to be able to
contact the first memory cell transistor and in a
corresponding manner for the second or the first row-
select/potential-equalization line to be able to
contact the second memory cell transistor. Each of the
10   two row-select/potential equalization lines can
therefore be used to contact the two memory cell
transistors adjacent to each other in one column of a
memory cell field. As a result of the inventive
arrangement of these two row-select/potential-
15   equalization lines, a high level of flexibility and
efficiency with respect to the contacting, i.e.,
potential equalization, of the memory cell transistors
can be achieved. At the same time, a significant
amount of space can be saved by the clever arrangement
20   of these row-select/potential-equalization lines, and
the arrangement of the other electrical lines required
for the semiconductor memory component can also be
designed in a much more highly simplified manner, so
that the programming of the semiconductor memory
25   component can be shifted chronologically to a point far
down the sequence of fabrication processes.

For potential equalization, it is advantageous for the
row-select/potential-equalization lines to be designed
30   to equalize the potentials present at a first and a
second word line. The gate region of the first memory
cell transistor is electrically connected to the first
word line, whereas the gate region of the second memory

cell transistor is connected electrically to the second
word line. The two row-select/potential-equalization
lines can be contacted by these word lines of the
memory cell transistors.

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It is preferable for the first and the second memory
cell transistor to be able to contact a data line,
which is designed in particular as a bit line, for the
programming of the memory states. The data line is
10   formed in a metallization plane which, seen from the
perspective of the memory cell transistors, lies above
the metallization planes in which the first and the
second row-select/potential-equalization lines are
located. The semiconductor memory component is thus
15   programmed after the row-select/potential-equalization
lines have been formed.

In another embodiment, the semiconductor memory
component has a memory cell field, in which a plurality
20   of memory cells is arranged in the form of a matrix.
The memory cell field has at least one first and one
second row; in both the first and the second rows there
is a plurality of memory cells, each with a memory cell
transistor. The memory cell transistors of the first
25   row are electrically connected to a first selection
line, and the memory cell transistors of the second row
are electrically connected to a second selection line.
The first selection line is electrically connected only
to the first row-select/potential-equalization line at
30   a distance of l memory cell transistors of the first
row. The second selection line is connected
electrically only to the second row-select/potential-
equalization line at a distance of k memory cell

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transistors of the second row. The whole numbers l and
k are much smaller than the total number of memory cell
transistors present in each case on the first and
second selection lines. It is possible, for example,

5   for the potential to be equalized on the word line over
a distance of 8 transistors of one row.

It is also possible for both the first and the second
word line to have at least one electrical connection to

10   the first row-select/potential-equalization line and an
electrical connection to the second row-
select/potential-equalization line. For example, the
first selection line or word line can be connected to
the first row-select/potential-equalization line after

15   l memory cell transistors of the first row and, for
example, to be electrically connected to the second
row-select/potential-equalization line after $2l$ memory
cell transistors of the first row. In analogous
fashion, the second selection line or word line can be

20   electrically connected to the second row-
select/potential-equalization line after k memory cell
transistors and to the first row-select/potential-
equalization line after $2k$ memory cell transistors.

25   In the case of a process according to the invention for
the production of a semiconductor memory component
which is designed in particular as a ROM component,
such as a mask-programmable ROM component, a first and
a second memory cell transistor are produced in a

30   substrate, and the first memory cell transistor is
electrically connected to a first selection line, and
the second memory cell transistor is electrically
connected to a second selection line, for example, a

first and a second word line. A first and a second
row-select/potential-equalization line are formed
vertically one above the other, between the two memory
cell transistors. As a result, a semiconductor memory
5   component with a much smaller space requirement can be
obtained.

In an advantageous exemplary embodiment, at least one
of the two row-select/potential-equalization lines is
10   designed to be equidistant from the two memory cell
transistors or from the two selection lines. The row-
select/potential-equalization line is thus arranged in
an especially space-saving manner, which is especially
advantageous for the following fabrication process.

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The amount of space required for the semiconductor
memory components can be considerably reduced in terms
of surface area and the turn-around-time can also be
significantly reduced because the programming of the
20   memory states can be performed at a relatively late
point in the fabrication process. In addition, the
arrangement of the other electrical lines required for
the semiconductor memory component can be optimized as
a result of the optimized arrangement of the row-
25   select/potential-equalization lines.

It is preferable for at least one of the two row-
select/potential-equalization lines to be centered
vertically above the diffusion region assigned to the
30   first and second memory cell transistors.

It is preferable for the first and the second row-
select/potential-equalization lines to be arranged one

above the other, so that they are coincident in the
vertical direction; the first and the second row-
select/potential-equalization lines can be formed in
different metallization planes. In particular, it is
5   possible for the first row-select/potential-
equalization line to be formed in a second or a third
metallization plane above the memory cell transistors
and for the second row-select/potential-equalization
line to be formed correspondingly in the third or
10   second metallization layer.

The semiconductor memory component can be programmed by
forming electrical contacts, especially by means of via
connections, with a data line produced in a fourth or
15   higher metallization plane. The data line, especially
a bit line, is formed in a metallization plane which is
produced above the metallization planes in which the
row-select/potential-equalization lines are produced.

20   As a result of the inventive arrangement and the
inventive formation of the row-select/potential-
equalization lines, it is possible to acquire an
additional programming plane, so to speak, in that
programming now takes place in a metallization plane
25   which is located above the metallization plane of the
row-select/potential-equalization lines and in
particular takes place in the last metallization plane
with a thin cross section. The "last thin
metallization plane" is the last metallization plane
30   required for the formation of the electrical lines
needed for the semiconductor memory component. Only
one or more comparatively thick metallization planes
are formed above this last thin metallization plane;

these thick planes are used for bonding the

semiconductor memory component, for example, or for

electrically connecting the semiconductor memory

component to the outside. Because these top or final

5   metallization planes are thicker than the first

metallization planes, they are no longer suitable as

programming planes.

10   BRIEF DESCRIPTION OF THE DRAWINGS

An exemplary embodiment of the invention is explained

in greater detail below on the basis of schematic

diagrams:

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Figure 1 shows a cross-sectional view of an

arrangement of two semiconductor memory components

designed according to the state of the art;

20   Figure 2 shows a cross-sectional view of another

design of a semiconductor memory component according to

the state of the art;

Figure 3 shows a plan view or layout of the

25   arrangement according to Figure 2;

Figure 4 shows a cross-sectional view of a

semiconductor component according to the invention; and

30   Figure 5 shows a plan view or layout of the

semiconductor memory component according to the

invention as shown in Figure 4.

DETAILED DESCRIPTION OF THE INVENTION

The same or functionally equivalent elements in the
figures are designated by the same reference numbers.

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Figure 2 shows another embodiment of a semiconductor
memory component according to the state of the art with
row-select/potential-equalization lines. In this known
memory cell design, a row-select/potential-equalization

10   line is assigned to each of the two memory cells SZ1
and SZ2 (unit cell characterized by the regions between
two separating lines TL). The row-select/potential-
equalization line PAW1 is assigned to the first memory
cell SZ1. The second row-select/potential-equalization

15   line PAW2 is provided in the second memory cell SZ2 and
is assigned exclusively to this memory cell SZ2. The
two row-select/potential-equalization lines PAW1 and
PAW2 are formed in the same metallization plane; in the
example shown here, they are formed in the second

20   metallization plane. The bit line BL in this exemplary
embodiment is located above the row-select/potential-
equalization lines PAW1 and PAW2.

To equalize the potentials present at the word lines W1

25   and W2, the word line W1 can be contacted only by the
row-select/potential-equalization line PAW1 formed in
the first memory cell SZ1. In similar fashion, the
word line W2 in the second memory cell SZ2 can be
contacted only by the second row-select/potential-

30   equalization line PAW2 formed in this memory cell SZ2.
On the basis of the applicable design rules
(lithography tools, component simulations, dopant
adjustments, chemical processing steps, optical
effects, use of different masks), by which the

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technology in question is characterized and which must

be taken into account in the development and production

of a semiconductor component of this type, the various

regions of the semiconductor component must be certain

5   distances apart. Depending on the corresponding

technology and the subregions being considered within a

semiconductor memory component between which it is

necessary to maintain a certain minimum distance, these

minimal distances specified by the design rules range

10   from a few hundredths to a few tenths of a μm.

In Figure 2, therefore, one of the minimum distances

which must be maintained is the distance a_1 between the

contact pad P2 in the first memory cell SZ1 and the

15   first line select/potential equalization line PAW1. In

addition, a minimum distance equivalent to one-half of

a_2 must also be maintained between the separating line

TL and the contact pad P2 of the first memory cell SZ1;

and a minimum distance equivalent to one-half of a_3

20   must be maintained between the second separating line

TL, forming the boundary of first memory cell SZ1, and

the first row-select/potential-equalization line PAW1.

The second memory cell SZ2 is designed in the same way

as the first memory cell SZ1, as a result of which a

25   total minimum distance a_3 is present between the two

row-select/potential-equalization lines PAW1 and PAW2.

These predetermined minimum distances a_1, a_2, and a_3,

which cannot be made any smaller than specified during

the development of the semiconductor memory component,

30   limit both the degree of miniaturization and thus also

the degree to which the amount of surface area required

for a semiconductor component can be reduced,

especially when two row-select/potential-equalization

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lines PAW1 and PAW2 are designed in the manner shown in
Figure 2.

Figure 3 shows a plan view or layout of the known
5   semiconductor memory component according to Figure 2.
Figure 2 represents a cross-sectional view of the
component along line AA of Figure 3. Figure 3 also
shows that the minimum distances a_3 and a_1, that is, the
minimum distance between the row-select/potential-
10   equalization lines PAW1 and PAW2 and the minimum
distance between each of the row-select/potential-
equalization lines PAW1 and PAW2 and the corresponding
contact pads P2, require a relatively large amount of
surface area on the semiconductor memory component. In
15   Figure 3, the contact pads P2 and P3 are drawn as
rectangular contact pads to simplify the diagram and to
make it easier to understand. In addition, Figure 3
also shows how the first row-select/potential-
equalization line PAW1 is contacted by the first word
20   line W1 of the first memory cell. The first row-
select/potential-equalization line PAW1 has a T-shaped
region oriented toward the word line W1; this region is
contacted by the word line via the two contact areas
KW1. In similar fashion, the second row-
25   select/potential-equalization line PAW2 is electrically
contacted by the second word line W2 of the second
memory cell via the contact areas KW2. The ground
potential equalization line PAM is contacted by the
common-diffusion region of the two memory cell
30   transistors via the contact area KPAM.

A semiconductor memory component according to the
invention in the form of a mask-programmable ROM

component is shown in cross section in Figure 4. Both
the first row-select/potential-equalization line PAW1,
i.e., the word line/potential-equalization line PAW1,
and the second row-select/potential-equalization line

5   PAW2, i.e., the word line/potential-equalization line
PAW2, are arranged symmetrically relative to the
separating line TL between the two memory cells SZ1 and
SZ2, above the common source region 50 of the memory
cell transistors. The two row-select/potential-

10 equalization lines PAW1 and PAW2 thus extend into more
than one memory cell, being located in part in both the
first and the second memory cell SZ1 and SZ2, and they
are essentially laterally equidistant from the word
lines WL1 and WL2. The first row-select/potential-

15 equalization line PAW1 is in the second metallization
plane, whereas the second row-select/potential-
equalization line PAW2 is in the third metallization
plane. For the potential equalization of the first
word line W1 ("wordline refresh"), it is thus possible

20 for electrical contact to be established both with the
first row-select/potential-equalization line PAW1 and
with the second row-select/potential-equalization line
PAW2.

25 In analogous fashion, a potential equalization
("wordline refresh") of the second word line W2 can be
achieved by forming an electrical connection with the
first PAW1 or with the second row-select/potential-
equalization line PAW2. As can be seen in Figure 4,

30 the minimum distance a_1, predetermined by the design
rules, namely, the distance between the contact areas
P2 and the first row-select/potential-equalization line
PAW1 and between the contact areas P3 and the second

row-select/potential-equalization line PAW2, must be maintained. As a result of the inventive arrangement of these row-select/potential-equalization lines PAW1 and PAW2, however, both the first memory cell SZ1 and

5   the second memory cell SZ2 can be reduced in size in the x-direction by half of the minimum distance a_3. The semiconductor memory component according to the invention shown in Figure 4 with the two memory cells SZ1 and SZ2 arranged next to each other in one column

10 can therefore be made smaller in the x-direction than the semiconductor memory component according to Figure 2 according to the state of the art by an amount equivalent to a width of an equalization line and the minimum design rule distance a_3.

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As a result of the vertical arrangement of the row-select/potential-equalization lines PAW1 and PAW2, it is also possible to reduce the size of the source region 50, which has a dimension d_2 in the lateral

20 direction in each of the first and second memory cells SZ1 and SZ2. This reduction in the lateral dimension of the source region 50 in each of the memory cells SZ1 and SZ2 from d_1 (Figure 2) to the lateral dimension d_2 (Figure 4) corresponds essentially to a half of the

25 minimum design rule distance a_3. As also shown in Figure 4, the drain region D1 and D2 of the memory cell transistors of the memory cells SZ1 and SZ2 are isolated from the adjacent drain regions of the adjacent transistors (not shown completely) by shallow

30 trench isolation areas STI. The memory cells in Figure 4 are programmed by forming via connections V3 to the bit line BL in the fourth metallization plane. In the exemplary embodiment shown here, the two memory cells,

i.e., the drain regions D1 and D2, are electrically
contacted by the bit line BL. The two memory cells SZ1
and SZ2 have a first logical state, which is called "0"
by convention. If, for example, the electrical
5   connection between the contact pad P3 and the bit line
BL were to be absent in the memory cell SZ1, that is,
if the via connection V3 had not been produced, this
memory cell SZ1 would have a second logical state,
namely the state called "1" by convention.

10

The contact areas K, the contact pads P1, P2, and P3,
and the via connections V1, V2, and V3 in the two
memory cells SZ1 and SZ2 are embedded and produced in
an isolation layer I, which can be designed as a multi-
15 layer system. The memory cells SZ1 and SZ2 can
therefore be programmed at the latest possible point
and especially in a metallization plane which is formed
as the last thin metallization plane in the stack of
layers built up in the y-direction. A metallization
20 plane of this type is referred to as "thin" when it has
a smaller or much smaller dimension in the y-direction
than the metallization planes formed above in it in the
positive y-direction. In the exemplary embodiment
according to Figure 4, it is also possible for the two
25 row-select/potential-equalization lines PAW1 and PAW2
to be coincident but asymmetric to the separating line
TL drawn between the two memory cells SZ1 and SZ2. It
must be remembered in this case that the minimum
distances a_1 to the contact pads P2 and P3 must always
30 be maintained (minimum design rule distances). In this
case, an arrangement would result which would have a
somewhat larger surface area than the design shown in
Figure 4, but it would still be considerably smaller

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than the designs according to the state of the art

shown in Figures 1 and 2.   It is also possible for the

row-select/potential-equalization lines PAW1 and PAW2

not to be coincident, that is, to be shifted in the x-

5   direction relative to each other (Figure 4).

As a result of the semiconductor memory component

according to the invention, therefore, programming can

be carried out at the latest possible point; in

10   particular, programming can be carried out in the last

thin metallization plane during the logic production

process.   Simultaneously, it is possible to achieve a

significant reduction in the amount of area required

for the semiconductor memory cells of the semiconductor

15   memory components.   It is also possible in Figure 4 for

the first row-select/potential-equalization line PAW1

to be provided in the first metallization plane, in

which the contact pads P1 are formed.   It is also

possible for the second row-select/equalization line

20   PAW2 to be formed in the second metallization plane, in

which the contact pads P2 are located.   The memory

cells SZ1 and SZ2 can then be contacted as early as the

third metallization plane, in which the bit line BL can

be formed.

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When the row-select/potential-equalization lines PAW1

and PAW2 are provided in the first and second

metallization planes, it is also possible, however, for

programming to be carried out in the fourth or higher

30   metallization plane.   In the exemplary embodiment

according to Figure 4, programming can also be carried

out in a higher plane than the fourth metallization

plane.   The essential point is that programming can be

accomplished in the last thin metallization plane. The
thick metallization planes located above - in the
positive y-direction - the last thin metallization
plane, i.e., the plane possibly used for the
5   programming of the memory cells, are designed for
establishing contact with bus lines or with the bus
system of an integrated circuit or for example, as
bonding planes. The thick metallization planes can
have a thickness in the y-direction which, for example,
10   is two-times or four-times greater than the thickness
of a thin metallization plane. The contact areas K,
the contact pads P1, and the ground potential
equalization line PAM can be made of tungsten, for
example. The via connections V1, V2, and V3; the
15   contact pads P2 and P3; and the two line
select/potential matching PAW1 and PAW2 between the
memory cells SZ1 and SZ2 can be made of copper, for
example. The bit line BL in the fourth metallization
plane can also be made of copper.
20

Figure 5 shows a plan view of the layout of the
inventive semiconductor component according to Figure
4. The two row-select/potential-equalization lines
PAW1 and PAW2 are arranged one above the other so that
25   they coincide with each other in the z-direction. In
the exemplary embodiment shown, the word line W1 is
contacted by the second row-select/potential-
equalization line PAW2 via the two contact areas KW1.
The second word line W2 is contacted by the first row-
30   select/potential-equalization line PAW1 via the contact
areas KW2. The word lines W1 and W2 can also be
contacted by the two row-select/potential-equalization
lines PAW1 and PAW2 in the reverse order. As can be

seen in Figure 5, the drain regions D1 and D2 and the

gate regions G1 and G2 of the memory cell transistors

are essentially the same in terms of surface area as

those in the diagram of Figure 3. The area of the

5   source region 50 assigned to the two memory cell

transistors, however, is greatly reduced. The size in

the x-direction of the two memory cell transistors

between the outer separating lines TL is reduced in

Figure 5, in comparison with the diagram in Figure 3,

10   by a width of an equalization line and the minimum

design rule distance a_3. The diagram in Figure 4

corresponds to a cross-sectional view along the line BB

(in Figure 5).

15   In the semiconductor memory component according to the

invention, especially a mask-programmable ROM

component, the row-select/potential-equalization lines

are, seen from the perspective of the memory cell

transistors, arranged vertically with respect to each

20   other and are located between the memory cell

transistors while extending into both of them at the

same time. The row-select/potential-equalization lines

are therefore arranged in such a way that they are

assigned to two memory cells arranged in one column of

25   a memory cell field. It is especially preferred for

the row-select/potential-equalization lines to be

nearly coincident with each other in separate planes

above the memory cell transistors and thus in the

middle and essentially centered between the diffusion

30   region assigned in common to the two memory cell

transistors. The two gate regions or word lines of the

memory cell transistors of the adjacent memory cells

can therefore be contacted by both row-

select/potential-equalization lines. Because the row-
select/potential-equalization line formed in one
metallization plane is centered above the diffusion
area assigned to both memory cell transistors of the
5   two adjacent memory cells, the area required for each
individual memory cell can be considerably reduced; in
particular, it can be reduced by at least a distance
equivalent to half of the minimum distance
predetermined by the design rules. In addition, as a
10   result of the inventive arrangement of the row-
select/potential-equalization lines in particular, the
arrangement of the word lines and of the bit lines can
be implemented in such a way that the memory cells can
be programmed at the latest possible point in the
15   fabrication process in a metallization plane designed
as the last thin metallization plane in the entire
stack of layers.

Although the invention has been illustrated and
20   described with respect to one or more implementations,
alterations and/or modifications may be made to the
illustrated examples without departing from the spirit
and scope of the appended claims. In addition, while a
particular feature of the invention may have been
25   disclosed with respect to only one of several
implementations, such feature may be combined with one
or more other features of the other implementations as
may be desired and advantageous for any given or
particular application. Furthermore, to the extent
30   that the terms "including", "includes", "having",
"has", "with", or variants thereof are used in either
the detailed description and the claims, such terms are
intended to be inclusive in a manner similar to the
term "comprising".
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